Method And Structure For Reducing Capacitance Between Interconnect Lines

ABSTRACT OF THE INVENTION

A method and structure for reducing capacitance between interconnect lines, characterized in that a pad oxide layer is added on each of metal lines over a substrate, having a plurality of semiconductor elements and one dielectric layer for isolating the semiconductor elements formed thereon, to form an interconnect line. The pad oxide layer added on each of metal lines increases intra-metal aspect ratio and facilitates air gap formation in each of the spacings between the adjacent interconnect lines having larger aspect ratios. Moreover, each of air gaps is formed below the pad oxide layer, while the top end and lower end thereof respectively exceed the top end and bottom end of the adjacent metal lines. The distance from the portion of the air gap between the top end and bottom end of the adjacent metal lines to the sidewall of the adjacent metal lines is more consistent and smaller. Therefore, a better low K effect between the adjacent metal lines is obtained.